

In the Claims:

Please amend the claims as indicated below.

1. (Previously presented) A method of compressing data that includes a sequence of at least two subsequent vectors, the at least two subsequent vectors each having one or more bits including care bits and don't care bits, the method comprising the steps of:

comparing corresponding bits of the two or more subsequent vectors to determine if they are compatible; and

responsive to determining that, for a number of said two or more vectors, all corresponding bits of the number of vectors are compatible,

filling in the don't care bits of the number of vectors using a random fill process when the number of vectors is less than a number n,

filling in the don't care bits of the number of vectors using a non-random fill process when the number of vectors is greater than or equal to the number n, and

merging the number of vectors to create a single merged vector representative thereof.

2. (Previously presented) A method according to claim 1, further comprising reconstructing the care bits of the number of vectors from the merged vector, wherein said data comprises test vector data for use in testing a logic product, and the method includes generating or obtaining original test vector data.

3. (Previously presented) A method according to claim 2, further comprising, responsive to determining that all corresponding bits of another number of the two or more subsequent vectors are not compatible, filling in the don't care bits of the other number of vectors using a random fill process, wherein said original test vector data is generated by means of an Automated Test Pattern Generation (ATPG) tool.

4. (Previously presented) A method according to claim 2, further comprising the step of generating a repeat value in respect of one or more merged vectors, said repeat value

being indicative of a number of times the respective merged vector should be repeated to reconstruct the care bits in the vectors of which the merged vector is representative.

5. (Original) A data set comprising test vector data for use in testing a logic product, said test vector data being compressed by the method of claim 4.

6. (Currently Amended) A method of testing a logic product, the method comprising the steps of generating compressed test vector data according to claim 5, reconstructing the test vector data by repeating the merged vector one or more times according to their respective repeat values, applying said reconstructed test vector data to an input of said logic product and obtaining the resultant output data.

7. (Previously presented) A method according to claim 6, further comprising the step of compressing said output data comprising a sequence of at least two subsequent output vectors, wherein an output vector comprises one or more bits, the method being characterized by the steps of:

comparing corresponding bits of two or more subsequent output vectors to determine if they are compatible; and

responsive to determining that all corresponding bits of said output vectors are compatible, merging said two or more output vectors to create a single output vector representative thereof.

8. (Currently amended) Apparatus for compressing data that includes a sequence of at least two subsequent vectors, the at least two subsequent vectors each having one or more bits including care bits and don't care bits, using the method according to claim 1 the apparatus comprising circuitry configured to

compare corresponding bits of the two or more subsequent vectors to determine if they are compatible; and

responsive to determining that, for a number of said two or more vectors, all corresponding bits of the number of vectors are compatible,

fill in the don't care bits of the number of vectors using a random fill process when the number of vectors is less than a number n,
fill in the don't care bits of the number of vectors using a non-random fill process when the number of vectors is greater than or equal to the number n, and
merge the number of vectors to create a single merged vector representative thereof.

9. (Previously presented) Apparatus according to claim 8, wherein said data comprises test vector data for use in testing a logic product.

10-12. (Cancelled).

13. (Previously presented) Apparatus according to claim 9, including an Automated Test Pattern Generation (ATPG) tool to generate original test vector data.

14. (Cancelled).

15. (Previously presented) Apparatus according to claim 9, including a memory to store merged vectors for use in testing the logic product.

16. (Cancelled).

17. (Previously presented) A method according to claim 1, wherein the non-random fill process proceeds by one or more of repeat fill or repetitive background data fill.

18. (Cancelled).

19. (Previously presented) A method according to claim 1, wherein the comparing and merging steps are repeated, resulting in a plurality of merged vectors.

20. (Previously presented) A method according to claim 19, wherein the merged vectors are arranged in a sequence of merged vector sets, each merged vector set having a first merged vector and a last merged vector, the method further comprising ordering the merged vector sets so that the last merged vector of one merged vector set is compatible with the first merged vector of the subsequent merged vector set.

21. (Previously presented) A method according to claim 20, further comprising merging the last merged vector of the one merged vector set with the first merged vector of the subsequent merged vector set.